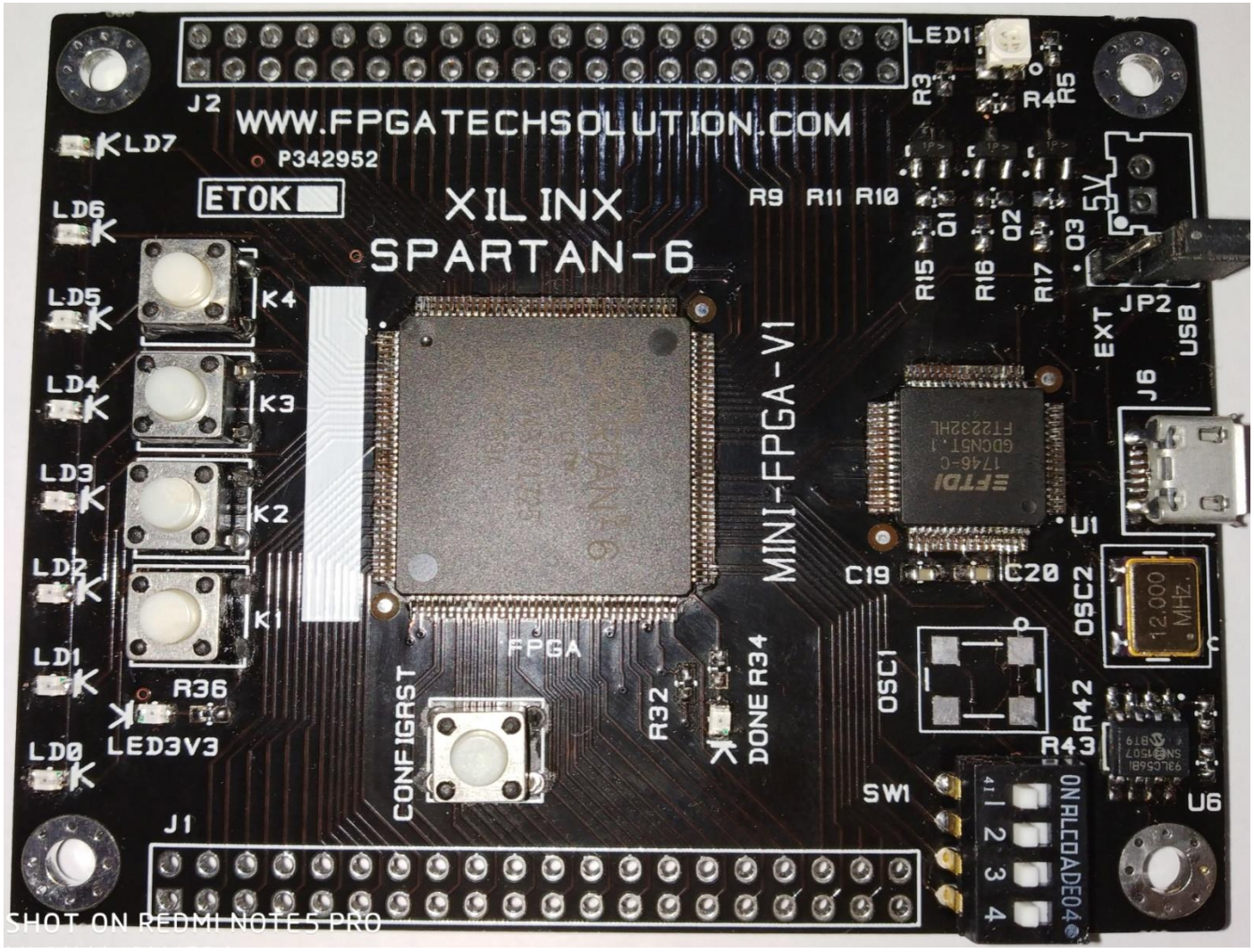
MANUAL MINI-SP6-FPGA

FPGA TECH SOLUTION

SOLUTION AHEAD



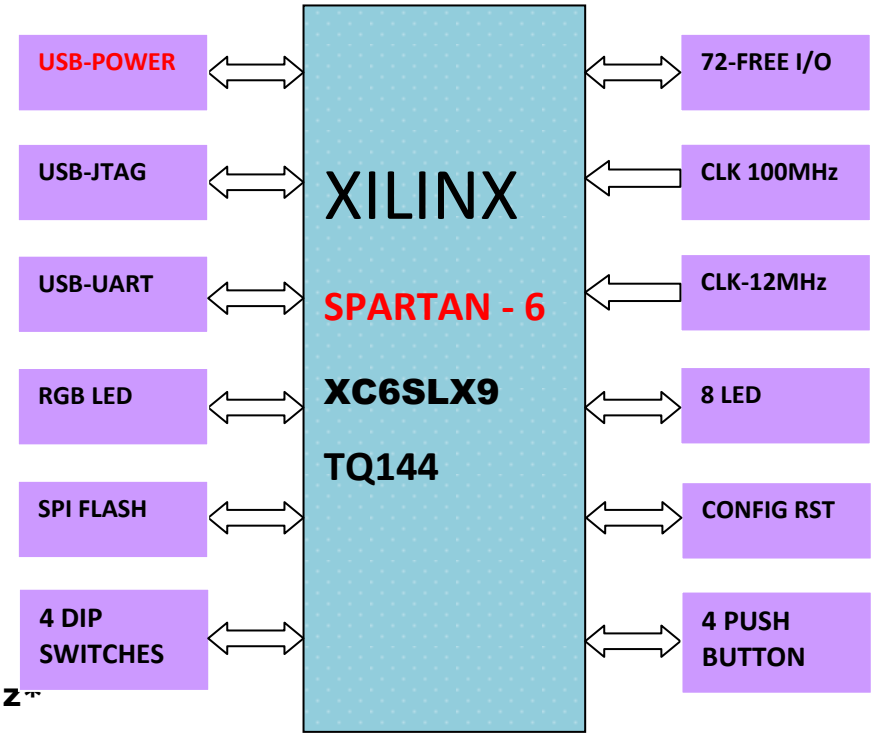
Key Features:

Spartan6-XC6SLX9_TQ144FPGA

- **Up to 102 user-I/O pins**
- **TQ-144 package**

Key components:

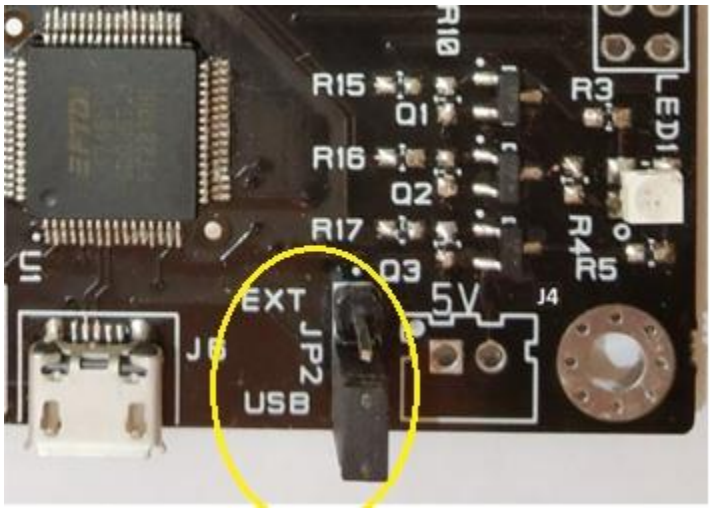
- **XC6SLX9_TQ144**
- **OSCILLATOR – 12MHz**
- **FLASH – M25P40**
- **USB POWER**
- **On board USB JTAG**
- **USB to SERIAL**
- **8 LED**
- **4 DIP SWITCHES**
- **4 PUSH BUTTONS**
- **72 USER I/O**
- **RGB – LED**
- **OSCILLATOR – 100MHz***

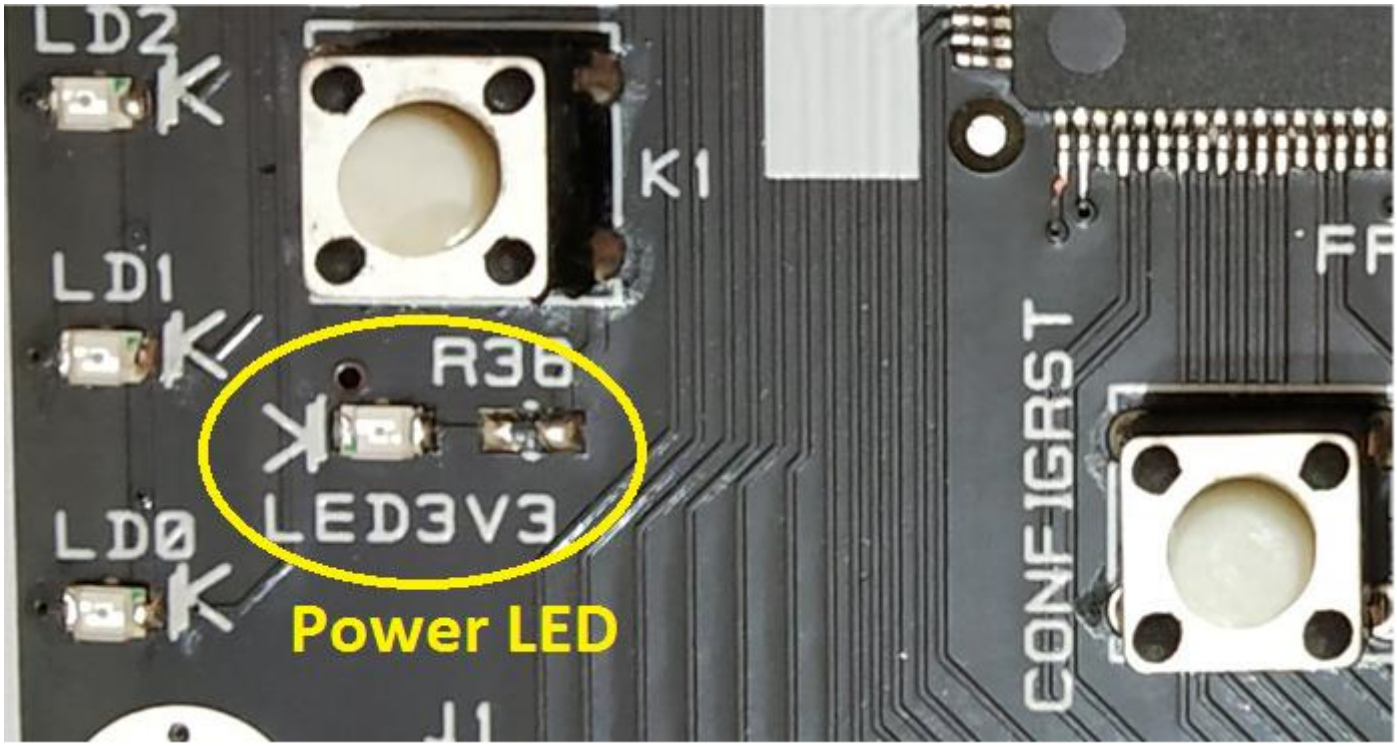


NOTE: 100 MHz oscillator is optional

BOARD POWERING

The **MINI-SP6-FPGA-V1** board can work on USB power; you can also connect external 5VDC supply. When **JP2** jumper is placed towards **USB** as shown in below image power is used from USB connector & when **JP2** jumper is placed towards **EXT** power is used from J4 connector (J4 is optional)

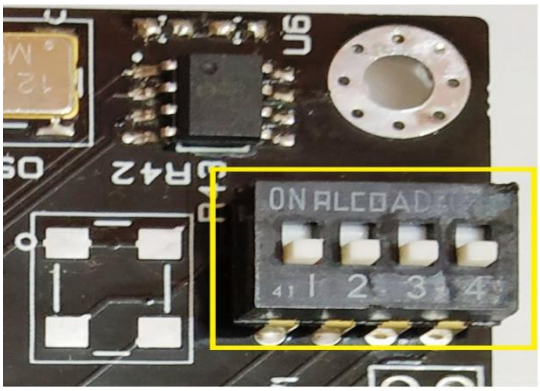




DIP Switches Interface

The **MINI-SP6-FPGA-V1** board has 4 push buttons & 4 DIP switch. Switches are used to provide digital input (i.e. logic 0 and logic 1).

Pin Assignment (UCF Location):



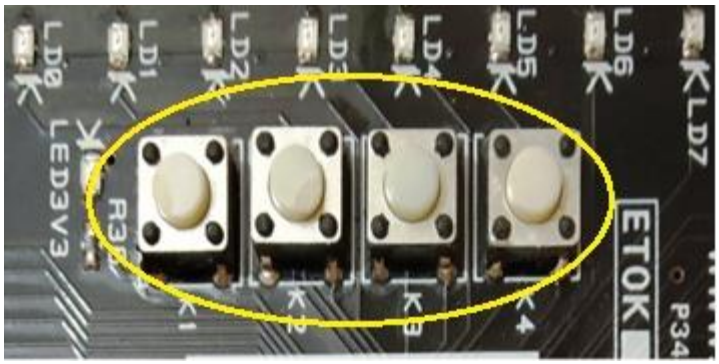
Slide Switch	XC6SLX9	Active
DIP_SW_1	P80	HIGH
DIP_SW_2	P81	HIGH
DIP_SW_3	P82	HIGH
DIP_SW_4	P83	HIGH

```
NET DIP_SW_1   LOC = P80 | IOSTANDARD = LVCMOS33;
NET DIP_SW_2   LOC = P81 | IOSTANDARD = LVCMOS33;
NET DIP_SW_3   LOC = P82 | IOSTANDARD = LVCMOS33;
NET DIP_SW_4   LOC = P83 | IOSTANDARD = LVCMOS33;
```

PUSH Button Interface

The **MINI-SP6-FPGA-V1** board has 4 push buttons & 4 DIP switch. Switches are used to provide digital input (i.e. logic 0 and logic 1).

Pin Assignment (UCF Location):



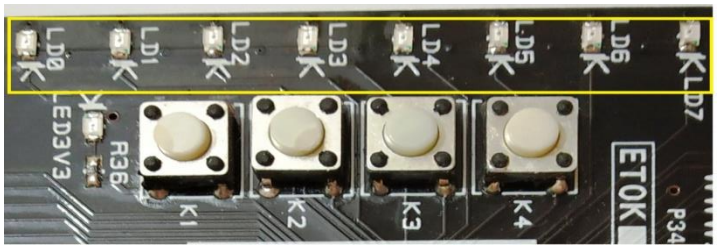
Slide Switch	XC6SLX9	Active
SW1	P17	HIGH
SW2	P14	HIGH
SW3	P10	HIGH
SW4	P7	HIGH

NET PUSH_BTN_1 LOC = P17 | IOSTANDARD = LVCMOS33;
NET PUSH_BTN_2 LOC = P14 | IOSTANDARD = LVCMOS33;
NET PUSH_BTN_3 LOC = P10 | IOSTANDARD = LVCMOS33;
NET PUSH_BTN_4 LOC = P7 | IOSTANDARD = LVCMOS33;

LED's Interface

The **MINI-SP6-FPGA-V1** board has 8 individual LED, A LED is assigned to each I/O to indicate its data status when I/O is configured as output. DIP switch is used to provide digital input (i.e. logic 0 and logic 1).

Pin Assignment (UCF Location):



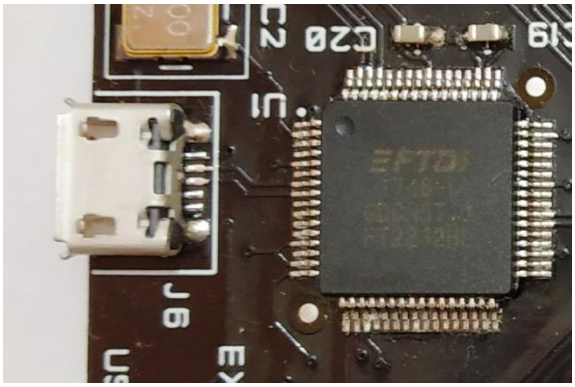
LED	XC6SLX9	Active
TL0	P16	HIGH
TL1	P15	HIGH
TL2	P12	HIGH
TL3	P11	HIGH
TL4	P9	HIGH
TL5	P8	HIGH
TL6	P6	HIGH
TL7	P5	HIGH

```
NET TL<0> loc=p16  | IOSTANDARD = LVCMOS33;
NET TL<1> loc=p15  | IOSTANDARD = LVCMOS33;
NET TL<2> loc=p12  | IOSTANDARD = LVCMOS33;
NET TL<3> loc=p11  | IOSTANDARD = LVCMOS33;
NET TL<4> loc=p9   | IOSTANDARD = LVCMOS33;
NET TL<5> loc=p8   | IOSTANDARD = LVCMOS33;
NET TL<6> loc=p6   | IOSTANDARD = LVCMOS33;
NET TL<7> loc=p5   | IOSTANDARD = LVCMOS33;
```

USB Interface

The **RNFDB SP6-V1**board have USB interface using device FT2232HL from FTDI. This act as USB to UART converter so that Communication with FPGA can accomplished by USB port.

Pin Assignment (UCF Location):



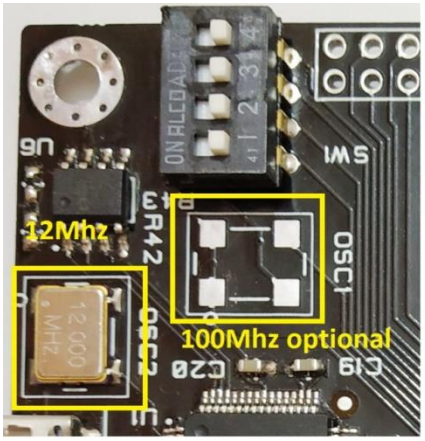
Signal Name	XC6SLX9
USB_Rx	P88
USB_TX	P85

```
NET USB_UART_RX  LOC = P88 | IOSTANDARD = LVCMOS33;
NET USB_UART_TX  LOC = P85 | IOSTANDARD = LVCMOS33;
```

Clock Sources

The **MINI-SP6-FPGA-V1** supports clock input sources which are listed below.
The board includes an on-board 12 MHz clock oscillator & 100 MHz clock oscillator (**optional**)

Pin Assignment (UCF Location):



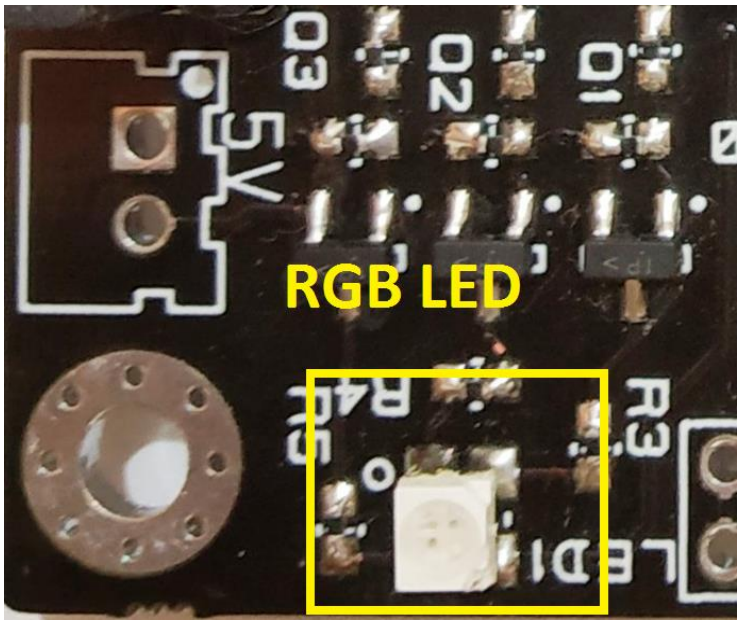
Signal Name	XC6SLX9
Clock 12Mhz	P87
Clock 100Mhz	P84

NET CLOCK_12MHZ LOC = P87 | IOSTANDARD = LVCMOS33;
NET CLOCK_100MHZ LOC = P84 | IOSTANDARD = LVCMOS33;

RGB-LED

The **MINI-SP6-FPGA-V1 has a RGB LED**

Pin Assignment (UCF Location):



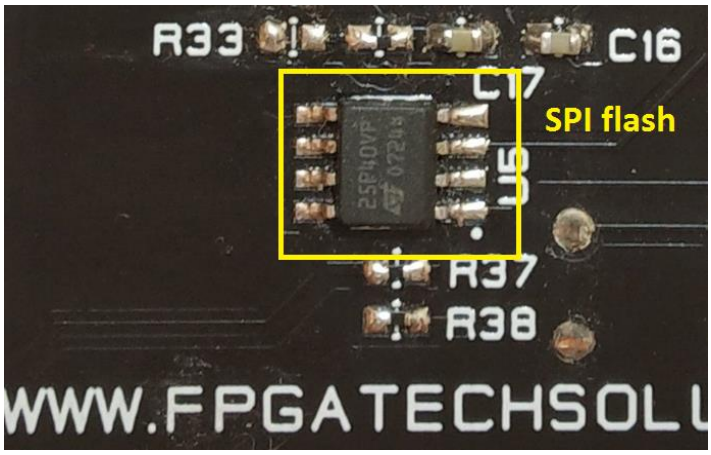
Signal Name	XC6SLX9
R	P93
G	P94
B	P95

```
NET LED_RED   LOC   = p95  | IOSTANDARD = LVCMOS33;
NET LED_GREEN LOC = p94  | IOSTANDARD = LVCMOS33;
NET LED_BLUE  LOC  = p93   | IOSTANDARD = LVCMOS33;
```

Flash interface

The **MINI-SP6-FPGA-V1 has a SPI flash interfaced with FPGA**

Pin Assignment (UCF Location):



Slide Switch	XC6SLX9
FLASH_CS	P38
MOSI	P64
MISO	P65
SPI_CLK	P70

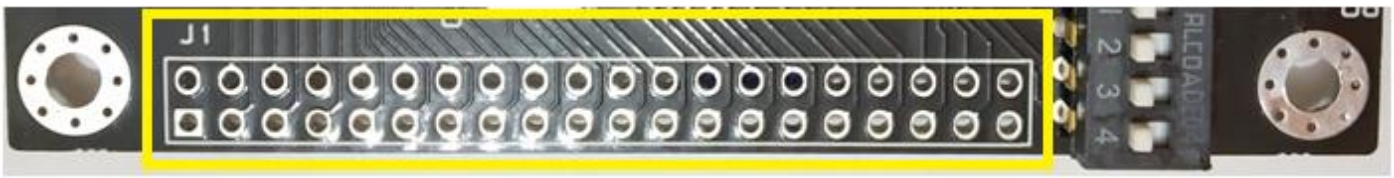
```
NET FLASH_CS   LOC = P38 | IOSTANDARD = LVCMOS33;
NET FLASH_MOSI LOC = P64 | IOSTANDARD = LVCMOS33;
NET FLASH_MISO LOC = P65 | IOSTANDARD = LVCMOS33;
NET FLASH_CLK  LOC = P70 | IOSTANDARD = LVCMOS33;
```

FREE INPUT OUTPUT

The **MINI-SP6-FPGA-V1** board has total 71 user I/O placed two input output connectors. J1 connector has 35 input output pins. J2 connector has 36 input output pins.

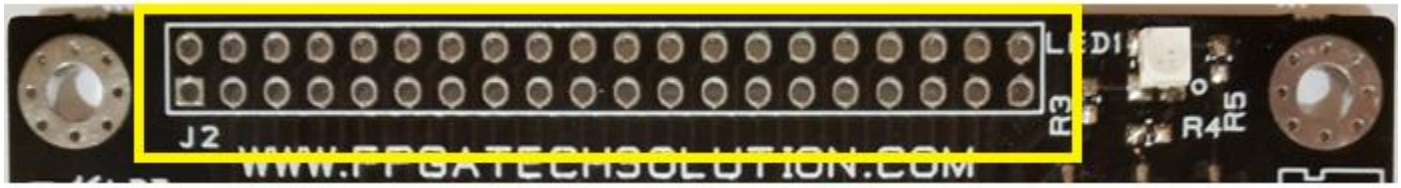
All pin can work with maximum 3.3V DC

Name	Signal Name	XCS6LX9-TQG144		Name	Signal Name	XCS6LX9-TQG144
	J1_1	**GND**			J1_2	**GND**
	J1_3	P22			J1_4	P21
	J1_5	P24			J1_6	P23
	J1_7	P27			J1_8	P26
	J1_9	P30			J1_10	P29
	J1_11	P33			J1_12	P32
	J1_13	P35			J1_14	P34
	J1_15	P41			J1_16	P40
	J1_17	P44			J1_18	P43
J1	J1_19	P46		**J1**	J1_20	P45
	J1_21	P48			J1_22	P47
	J1_23	P51			J1_24	P50
	J1_25	P56			J1_26	P55
	J1_27	P58			J1_28	P57
	J1_29	P61			J1_30	P59
	J1_31	P66			J1_32	P62
	J1_33	P67			J1_34	**NC**
	J1_35	P75			J1_36	P74
	J1_37	P79			J1_38	P78
J1	J1_39	+3.3V		**J1**	J1_40	+3.3V



```
NET IO_J1_3  LOC =  P22  | IOSTANDARD = LVCMOS33;
NET IO_J1_4  LOC =  P21  | IOSTANDARD = LVCMOS33;
NET IO_J1_5  LOC =  P24  | IOSTANDARD = LVCMOS33;
NET IO_J1_6  LOC =  P23  | IOSTANDARD = LVCMOS33;
NET IO_J1_7  LOC =  P27  | IOSTANDARD = LVCMOS33;
NET IO_J1_8  LOC =  P26  | IOSTANDARD = LVCMOS33;
NET IO_J1_9  LOC =  P30  | IOSTANDARD = LVCMOS33;
NET IO_J1_10 LOC = P29  | IOSTANDARD = LVCMOS33;
NET IO_J1_11 LOC = P33  | IOSTANDARD = LVCMOS33;
NET IO_J1_12 LOC = P32  | IOSTANDARD = LVCMOS33;
NET IO_J1_13 LOC = P35  | IOSTANDARD = LVCMOS33;
NET IO_J1_14 LOC = P34  | IOSTANDARD = LVCMOS33;
NET IO_J1_15 LOC = P41  | IOSTANDARD = LVCMOS33;
NET IO_J1_16 LOC = P40  | IOSTANDARD = LVCMOS33;
NET IO_J1_17 LOC = P44  | IOSTANDARD = LVCMOS33;
NET IO_J1_18 LOC = P43  | IOSTANDARD = LVCMOS33;
NET IO_J1_19 LOC = P46  | IOSTANDARD = LVCMOS33;
NET IO_J1_20 LOC = P45  | IOSTANDARD = LVCMOS33;
NET IO_J1_21 LOC = P48  | IOSTANDARD = LVCMOS33;
NET IO_J1_22 LOC = P47  | IOSTANDARD = LVCMOS33;
NET IO_J1_23 LOC = P51  | IOSTANDARD = LVCMOS33;
NET IO_J1_24 LOC = P50  | IOSTANDARD = LVCMOS33;
NET IO_J1_25 LOC = P56  | IOSTANDARD = LVCMOS33;
NET IO_J1_26 LOC = P55  | IOSTANDARD = LVCMOS33;
NET IO_J1_27 LOC = P58  | IOSTANDARD = LVCMOS33;
NET IO_J1_28 LOC = P57  | IOSTANDARD = LVCMOS33;
NET IO_J1_29 LOC = P61  | IOSTANDARD = LVCMOS33;
NET IO_J1_30 LOC = P59  | IOSTANDARD = LVCMOS33;
NET IO_J1_31 LOC = P66  | IOSTANDARD = LVCMOS33;
NET IO_J1_32 LOC = P62  | IOSTANDARD = LVCMOS33;
NET IO_J1_33 LOC = P67  | IOSTANDARD = LVCMOS33;
NET IO_J1_35 LOC = P75  | IOSTANDARD = LVCMOS33;
NET IO_J1_36 LOC = P74  | IOSTANDARD = LVCMOS33;
NET IO_J1_37 LOC = P79  | IOSTANDARD = LVCMOS33;
NET IO_J1_38 LOC = P78  | IOSTANDARD = LVCMOS33;
```

Name	Signal Name	XCS6LX9-TQG144		Name	Signal Name	XCS6LX9-TQG144
	J2_1	**GND**			J2_2	**GND**
	J2_3	P1			J2_4	P2
	J2_5	P143			J2_6	P144
	J2_7	P141			J2_8	P142
	J2_9	P139			J2_10	P140
	J2_11	P137			J2_12	P138
	J2_13	P13			J2_14	P134
	J2_15	P131			J2_16	P132
	J2_17	P126			J2_18	P127
J2	J2_19	P123		**J2**	J2_20	P124
	J2_21	P120			J2_22	P121
	J2_23	P118			J2_24	P119
	J2_25	P116			J2_26	P117
	J2_27	P114			J2_28	P115
	J2_29	P111			J2_30	P112
	J2_31	P104			J2_32	P105
	J2_33	P101			J2_34	P102
	J2_35	P99			J2_36	P100
	J2_37	P97			J2_38	P97
J2	J2_39	**+3.3V**		**J2**	J2_40	**+3.3V**



```
NET IO_J2_3  LOC = P1     | IOSTANDARD = LVCMOS33;
NET IO_J2_4  LOC = P2     | IOSTANDARD = LVCMOS33;
NET IO_J2_5  LOC = P143   | IOSTANDARD = LVCMOS33;
NET IO_J2_6  LOC = P144   | IOSTANDARD = LVCMOS33;
NET IO_J2_7  LOC = P141   | IOSTANDARD = LVCMOS33;
NET IO_J2_8  LOC = P142   | IOSTANDARD = LVCMOS33;
NET IO_J2_9  LOC = P139   | IOSTANDARD = LVCMOS33;
NET IO_J2_10 LOC = P140 | IOSTANDARD = LVCMOS33;
NET IO_J2_11 LOC = P137 | IOSTANDARD = LVCMOS33;
NET IO_J2_12 LOC = P138 | IOSTANDARD = LVCMOS33;
NET IO_J2_13 LOC = P133 | IOSTANDARD = LVCMOS33;
NET IO_J2_14 LOC = P134 | IOSTANDARD = LVCMOS33;
NET IO_J2_15 LOC = P131 | IOSTANDARD = LVCMOS33;
NET IO_J2_16 LOC = P132 | IOSTANDARD = LVCMOS33;
NET IO_J2_17 LOC = P126 | IOSTANDARD = LVCMOS33;
NET IO_J2_18 LOC = P127 | IOSTANDARD = LVCMOS33;
NET IO_J2_19 LOC = P123 | IOSTANDARD = LVCMOS33;
NET IO_J2_20 LOC = P124 | IOSTANDARD = LVCMOS33;
NET IO_J2_21 LOC = P120 | IOSTANDARD = LVCMOS33;
NET IO_J2_22 LOC = P121 | IOSTANDARD = LVCMOS33;
NET IO_J2_23 LOC = P118 | IOSTANDARD = LVCMOS33;
NET IO_J2_24 LOC = P119 | IOSTANDARD = LVCMOS33;
NET IO_J2_25 LOC = P116 | IOSTANDARD = LVCMOS33;
NET IO_J2_26 LOC = P117 | IOSTANDARD = LVCMOS33;
NET IO_J2_27 LOC = P114 | IOSTANDARD = LVCMOS33;
NET IO_J2_28 LOC = P115 | IOSTANDARD = LVCMOS33;
NET IO_J2_29 LOC = P111 | IOSTANDARD = LVCMOS33;
NET IO_J2_30 LOC = P112 | IOSTANDARD = LVCMOS33;
NET IO_J2_31 LOC = P104 | IOSTANDARD = LVCMOS33;
NET IO_J2_32 LOC = P105 | IOSTANDARD = LVCMOS33;
NET IO_J2_33 LOC = P101 | IOSTANDARD = LVCMOS33;
NET IO_J2_34 LOC = P102 | IOSTANDARD = LVCMOS33;
NET IO_J2_35 LOC = P99  | IOSTANDARD = LVCMOS33;
NET IO_J2_36 LOC = P100 | IOSTANDARD = LVCMOS33;
NET IO_J2_37 LOC = P97  | IOSTANDARD = LVCMOS33;
NET IO_J2_38 LOC = P98  | IOSTANDARD = LVCMOS33;
```